

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 60-144026

(43)Date of publication of application : 30.07.1985

(51)Int.Cl.

H03M 13/12

(21)Application number : 59-000651

(71)Applicant : FUJITSU LTD

(22)Date of filing :

06.01.1984

(72)Inventor : YAMASHITA ATSUSHI

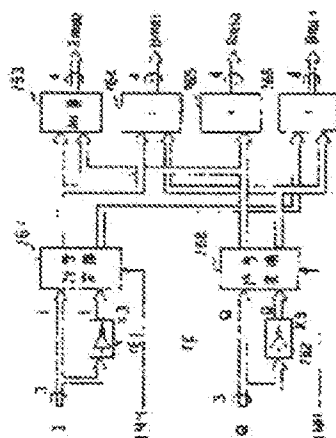
KATO TADAYOSHI

(54) VITERBI DECODER

(57)Abstract:

PURPOSE: To inhibit a metric calculation to a dummy bit without increasing a circuit scale by providing a code converting part for converting an inversion and a non-inversion of a receiving code by receiving a metric calculation inhibiting signal, on a branch metric calculating circuit.

CONSTITUTION: At the time of a branch metric calculation, a code is converted immediately before adding a code, dummy bits QR and -QR are set to the same value, and an equal effect to that which has inhibited a metric calculation is given. Code converting parts 767, 768 are added to a branch metric calculating part 76. The code converting part



767 converts a code so as to be $I=-I$ only when a metric calculation inhibiting signal INH from a dummy bit inserting part is active, and outputs I and $-I$ as they are in other case. The code converting part 768 also executes the same. The dummy bit inserting part knows an inserting position of a dummy bit, therefore, the inhibiting signal INH to be inputted to the code converting parts 767, 768 from said part can be generated easily.